SUMMER SCHOOL

ON

VLSI DIGITAL LOGIC DESIGN AND SYNTHESIS FOR FPGA (ONLINE MODE)

JULY 14 – JULY 19, 2025

COURSE DURATION: 6 DAYS

SKILLS TARGETED

- **BE/BTECH IN**
- **COMPUTER SCIENCE AND ENGINEERING**
- **ELECTRONICS AND COMMUNICATION ENGINEERING,**
- **ELECTRICAL ENGINEERING,**
- **ELECTRONICS AND INSTRUMENTATION ENGINEERING.**

- **PG DIPLOMA/MS/MSC IN**

ELECTRONICS OR ELECTRONICS DESIGN

- **ITI IN**

ELECTRONICS DESIGN

I.INTRODUCTION AND VLSI DESIGN REPRESENTATION (DAY 1):

- **VLSI DESIGN CYCLE - FRONT END DESIGN FLOW & BACKEND DESIGN FLOW**
- **FPGA DESIGN FLOW**
- **DESIGN STYLES AND HDL LANGUAGE FEATURES**
- **OPERATORS AND MODELING EXAMPLES**
- **DESCRIPTION STYLES**

II. COMBINATIONAL LOGIC DESIGN (DAY 2 – DAY 3):

- **PROCEDURAL ASSIGNMENT AND EXAMPLES: ADDER, SUBTRACTOR, MULTIPLIER, COMPARATOR, MULTIPLEXING, DEMULTIPLEXING, ENCODERS, DECODERS, PARITY CHECKERS**

III. SEQUENTIAL LOGIC DESIGN (DAY 4 - DAY 5):

- **SYNCHRONOUS LOGIC DESIGN, FLIP-FLOPS, COUNTERS, REGISTERS MODELING FINITE STATE MACHINES.**

IV. DIGITAL SYSTEM DESIGN (DAY 6):

- **I2C/UART PROTOCOL DESIGN.**

SCAN & PAY

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Registration fee is Rs. 2360 (Including 18% GST)

Registration form link: https://forms.gle/1pEov7U9j87Hk6do9